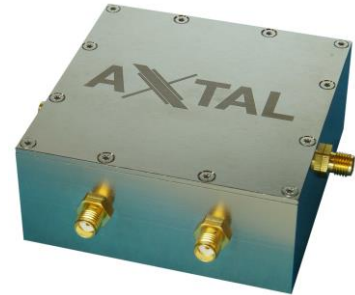


<b>Specification</b>	<b>AXPLO2700</b>	Rev.: 2	Date: 2021-01-26
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**Oscillator type:** Fully customizable UHF/SHF PLL frequency source  
Phase-Locked Ultra-Low Phase Noise OCXO (PLOCXO)  
with multiple outputs

**Features:**

- Fully customizable phase-locked frequency source
- Multiple phase coherent outputs with 1 direct OCXO output and up to 2 user-definable multiplied outputs
- Internal Ultra-Low Phase Noise Reference OCXO locked to external reference
- Supreme OCXO with -180 dBc/Hz noise floor
- Wide input reference frequency range



Parameter	min.	typ.	max.	Unit	Condition
Reference frequency (input) $f_{REF}$	10		150	MHz	
OCXO output frequency range	50		160	MHz	
Multiplied output frequency range	100		7000	MHz	Customizable (Note 2, 3)
<b>Frequency stability (free-running)</b>					
frequency tolerance		±100		ppb	
over operating temperature range		±100		ppb	
Long term (aging) per year		±100		ppb	after 30 days operation
<b>Reference input</b>					
PLL Performance	Tailored to your requirements				(Note 4)
<b>OCXO RF output</b>					
Signal waveform	Sine wave				
Load $R_L$	50			$\Omega$	±5%
Output level		+10		dBm	
Harmonics		-40		dBc	
Spurious			-90	dBc	
Phase noise	Consult factory Best close-in phase noise available Noise floor -180 dBc/Hz				(Note 4)
<b>Multiplied RF outputs</b>					
Customizable outputs	3				Phase coherent to OCXO
Signal waveform	Sine wave				
Load $R_L$	50			$\Omega$	±5%
Output level		+13		dBm	
Harmonics		-50		dBc	
Sub-harmonics (multiples of RF1)		-50		dBc	
Spurious			-90	dBc	
Phase noise	Consult factory				
<b>Warm-up time @ +25°C</b>			5	min	$\Delta f_{final}/f_0 < \pm 0.1$ ppm
<b>Supply voltage <math>V_s</math></b>	10		15	V	
<b>Operating temperature range</b>	-10		+60	°C	Other range on request

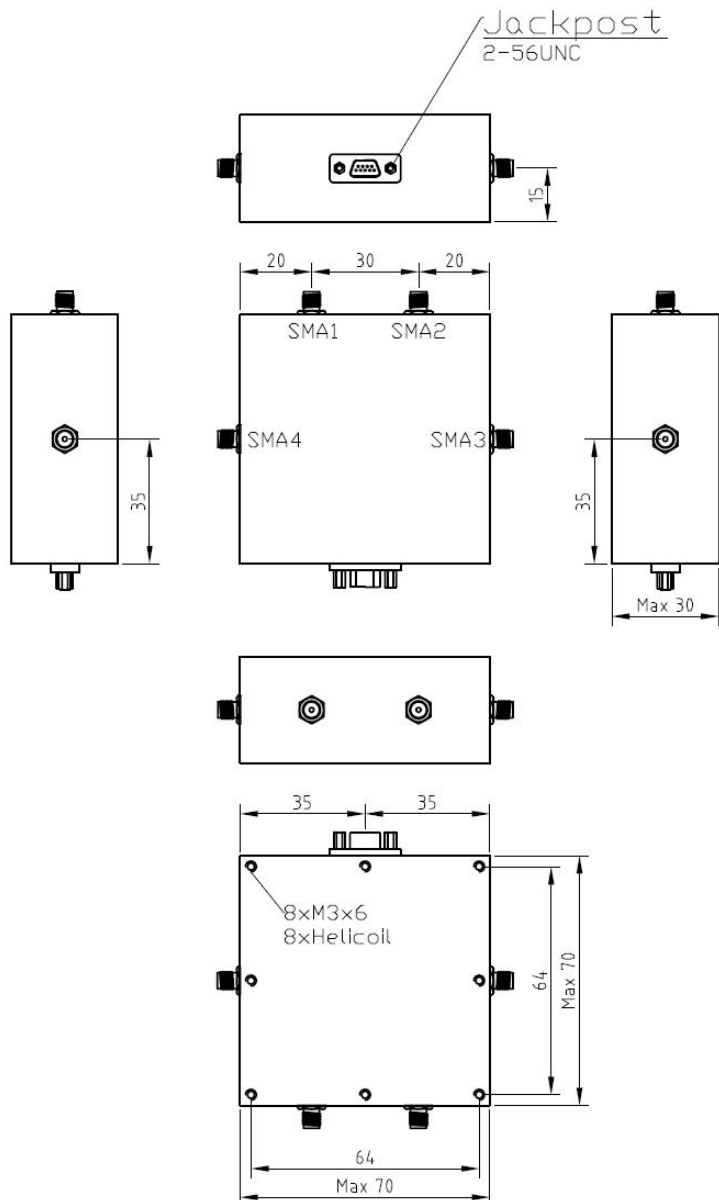
**- See Performance Examples below -**

Parameter	min.	typ.	max.	Unit	Condition
Enclosure (see drawing) (LxWxH)	70x70x30 max.			mm	
Weight			200	g	

**Notes:**

1. Terminology and test conditions are according to IEC60679-1 and MIL-PRF-55310, unless otherwise stated
2. Multiplied frequencies must be an integer multiple of OCXO frequency
3. Fully customizable to your requirements. Please consult factory for performance levels.
4. PLL Design in accordance with your phase-noise performance requirements

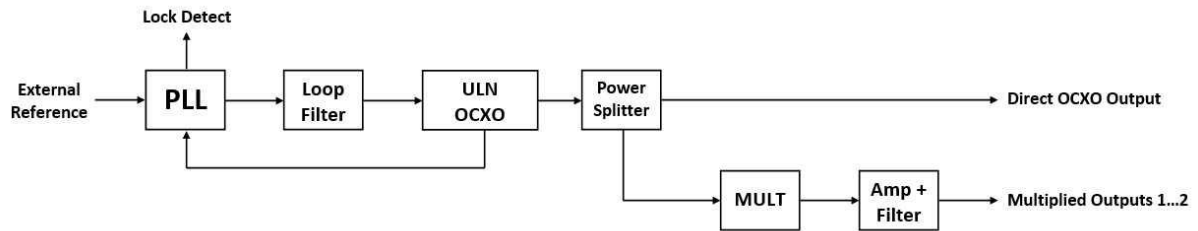
**Enclosure drawing**



**Micro-D Connector:** M83513/03 with jack posts M83513/05-07 (2-56 UNC)

**Feedthrough connectors on request – Unused outputs will be blind screwed**

### General block diagram

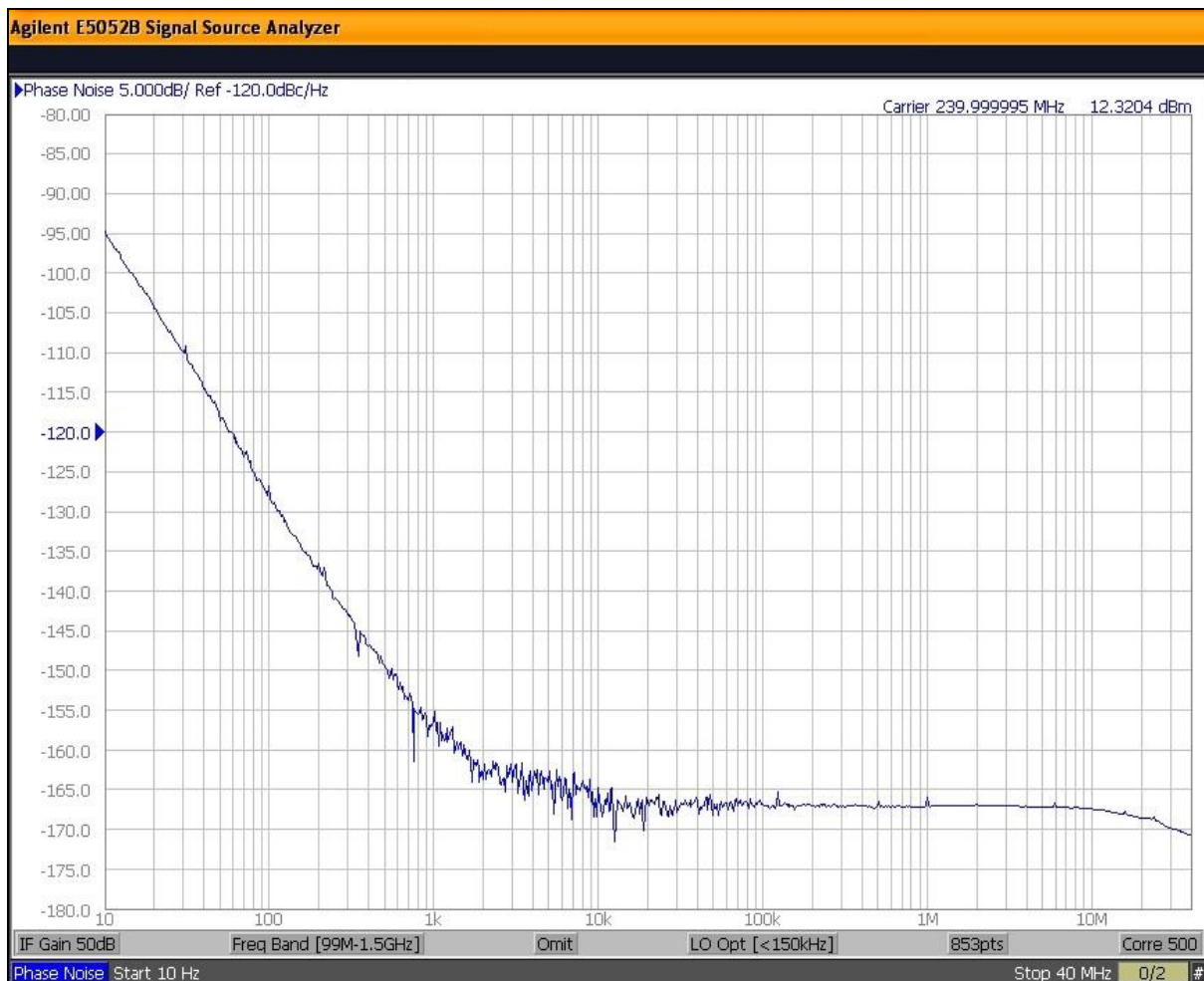


\* For improved noise floor and very low sub-harmonic content SAW filters can be used.

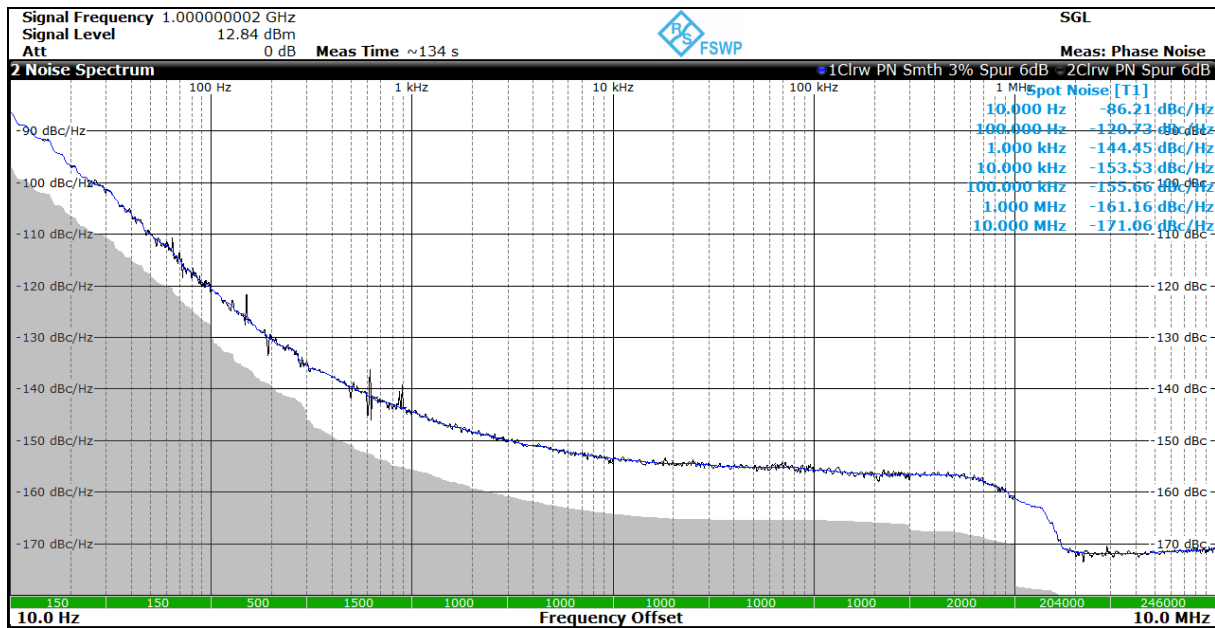
### Performance Examples

#### (1) 240 MHz Output (Multiplication x2)

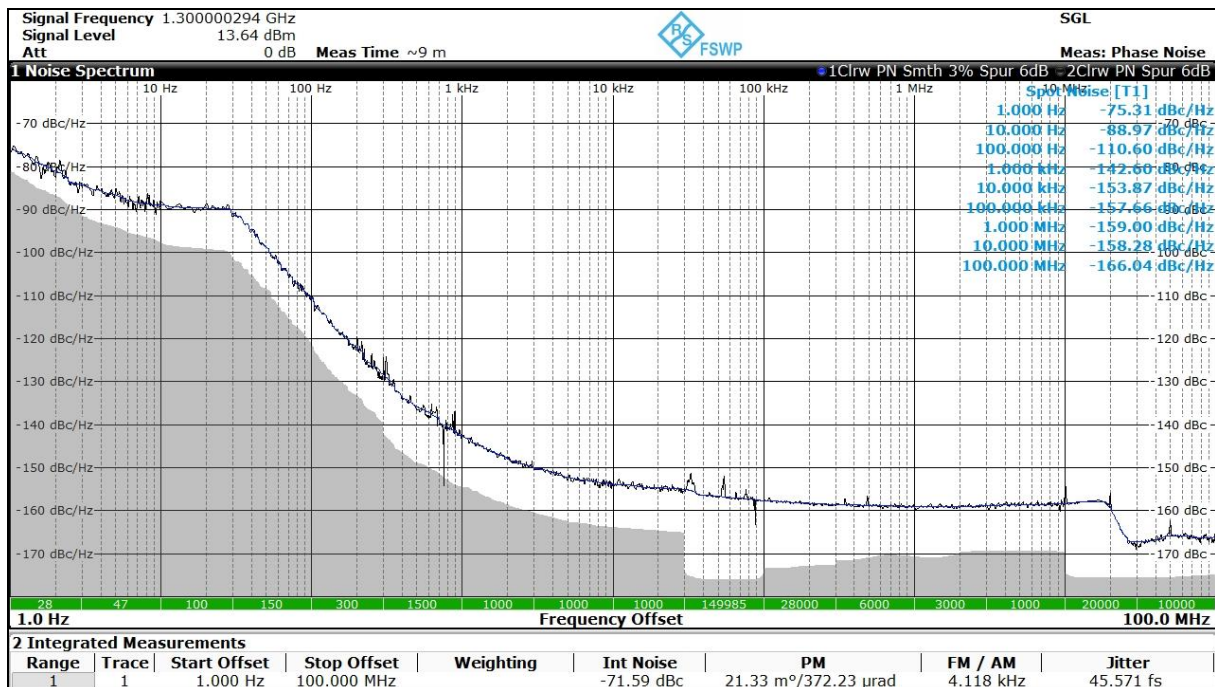
Locked to Ultra-Low Noise 10 MHz Reference (Loop Filter <10 Hz)



**(2) 1 GHz Output (Multiplication x10 including SAW Filter)**  
**Locked to Ultra-Low Noise 10 MHz Reference (Loop Filter <10 Hz)**



**(3) 1.3 GHz Output (Multiplication x10 including SAW Filter)**  
**Locked to Ultra-Low Noise 10 MHz Reference for ultra-low jitter**



**Revision History**

Rev.	Drawing	Date [dd.mm.yyyy]	Remarks	Author	Checked
1	D0	19.08.2016	First issue	HH	ME
2	D0	30.10.2018	Changed to fully customizable model	HH	ME
2	D1	26.01.2021	Drawing updated, performance examples added	HH	HH