

**APPLICATION NOTE AXAN-011****Handling and Testing of Crystal Oscillators**

This application note provides answers to some frequently addressed issues related to the testing of crystal oscillators.

For more details about test and measurement methods of crystal oscillators please refer to IEC standard 60679-1 and to MIL-PRF-55310.

**1. ESD (Electrostatic Sensitive Devices) Handling**

Crystal oscillators are electrostatic sensitive devices. Direct touching of the terminals with the fingers must be avoided. Proper handling according to the established ESD handling rules as in IEC 61340-5-1 and EN 100015-1 is mandatory to avoid degradations of the oscillator performance due to damages of the internal circuitry by electrostatics. If not otherwise stated, our oscillators meet the requirements of the Human Body Model (HBM) according to IEC 61000-4-2

**2. Handling**

Excessive mechanical shocks during handling as well as manual and automatic assembly have to be avoided. If the oscillator was unintentionally dropped or otherwise subject to strong shocks, it should be verified that the electrical function is still within specification.

**3. Power supply**

To avoid uncontrolled potentials, crystal oscillators should be powered up only after all terminals are connected properly. "Hot plug-in" into a fixture which is already connected to the supply power must be avoided. Wrong polarity or excessive supply voltage can cause a permanent damage of the oscillator.

It is highly recommended to add one or two blocking capacitors with shortest possible wiring between the DC power input (VCC) terminal and the ground (GND) terminal of the oscillator. Typical values are 10 nF (X7R) and 100 pF (COG). An additional bulk capacitor in the  $\mu$ F range may be inserted anywhere on the board. Good engineering practice is to use ground and supply voltage planes on the (multilayer) printed circuit board.

**4. RF Output**

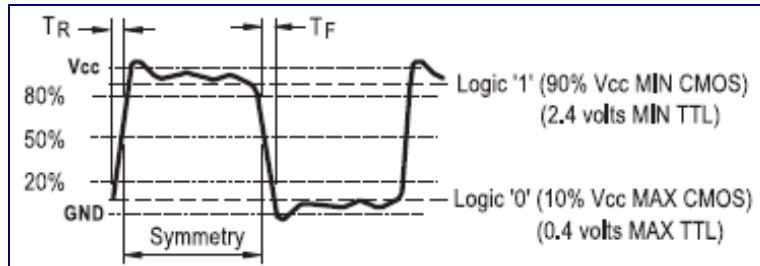
The RF Output has to be terminated with the specified load as follows.

**a. Sine wave output with 50  $\Omega$  termination**

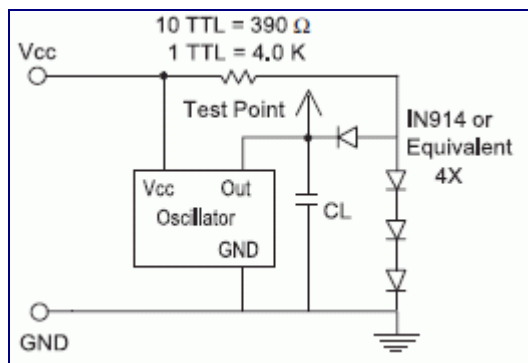
The 50  $\Omega$  termination should either be connected directly at the RF output terminal or at the end of a 50  $\Omega$  coaxial cable.

If multiple connections (e.g. to oscilloscope or power meter and frequency counter) are required, a 50 Ω power splitter or a coupler should be used. For accurate amplitude measurement it must be assured that the input impedance of the test instrument is accurately 50 Ω with a VSWR within the specified limits. This is not necessarily the case for some oscilloscopes and frequency counters. In that case a 10 dB attenuator should be inserted at the instrument input.

**b. Single square wave (logic) outputs**

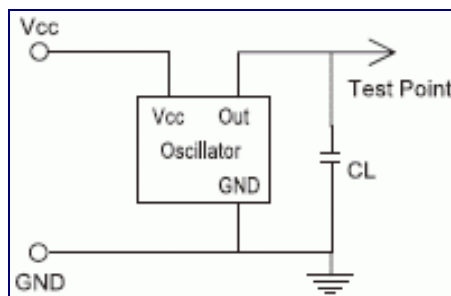


**i. TTL output**



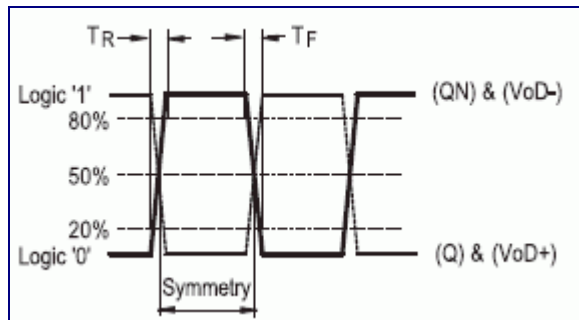
CL = 5 pF per gate (fan-out). It includes the input capacitance of the probe or oscilloscope

**ii. (H)CMOS and LVCMOS output**

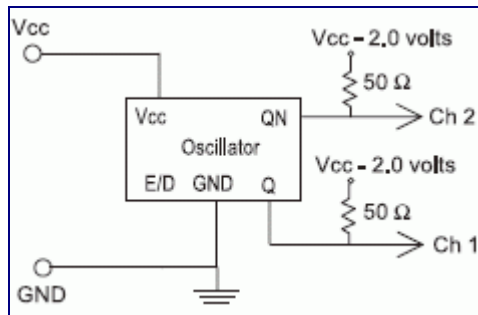


CL = 15 pF or 50 pF, depends on the specification. It includes the input capacitance of the probe or oscilloscope

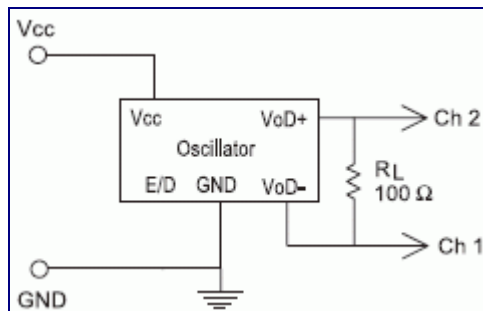
**c. Two Complementary square wave outputs**



**i. PECL output**



**ii. LVDS output**



Note:

Coaxial cables, which are not terminated with their nominal impedance (usually 50 Ω) will cause distortion and degradation of the output signal because of two reasons

- Impedance mismatch generates reflections, which are causing distortion of the waveform. The impact is in particular dramatic for square-wave logic output signals.
- A non-terminated coaxial cable shows an input impedance about 100 pF per meter capacitance to ground (as long as the cable length is small compared to a quarter wavelength). This capacitance in connection with the input capacitance of the connected device (e.g. test instrument) creates a capacitive overload condition, which distorts and degenerates the output voltage.

## 5. Electronic Frequency Control (EFC)

Crystal oscillators which are providing means for Electronic Frequency Control (EFC) must be properly connected to assure operation at the nominal frequency within the specified tolerances. In any case it should be avoided to leave the EFC (VC) input floating.

### a. External Control Voltage

If the EFC input is fed by an external DC control voltage, care must be taken, that ground loops with the DC supply current are avoided by directly applying the control voltage between the VC and the Ground (GND) terminal of the oscillator.

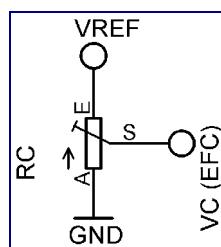
Note:

Excessive noise of the EFC supply may degrade the phase noise and jitter performance of the RF signal. Therefore batteries or very low noise DC supplies are necessary for accurate phase noise and jitter measurements.

### b. External Potentiometer

If an external potentiometer is used for frequency control, its resistance should be lower than the input impedance of the EFC (VC) input by a factor of at least five.

Certain oscillators (TCXO and OCXO) provide a separate reference voltage output (VREF) terminal for supplying the frequency control potentiometer. This reference voltage has low noise and its stability over temperature is factored in the temperature compensation process during manufacturing. The connection scheme is shown below.



The resistance value of the potentiometer RC must be chosen such, that the maximum allowed current drain of the VREF output (usually < 1 mA) is not exceeded.

Mosbach, 03 November 2008  
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